JC17 Rec'd PCT/PTO 13 JUL 2001

FORM PTO-1390 (Modified) (REV 11-2000) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE		ATTORNEY'S DOCKET NUMBER
TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. 371		83256
		U.S. APPLICATION NO. (IF KNOWN, SEE 37 CFR 09/889260
INTERNATIONAL APPLICATION NO. **PCT/DE00/00021**	INTERNATIONAL FILING DATE **January 3, 2000**	PRIORITY DATE CLAIMED **January 21, 1999**

TITLE OF INVENTION
ELECTRONIC PHASE-LOCKED LOOP

APPLICANT(S) FOR DO/EO/US
Infineon Technologies AG

Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:

1. ☒ This is a **FIRST** submission of items concerning a filing under 35 U.S.C. 371.
2. ☐ This is a **SECOND** or **SUBSEQUENT** submission of items concerning a filing under 35 U.S.C. 371.
3. ☐ This is an express request to begin national examination procedures (35 U.S.C. 371(f)). The submission must include itens (5), (6), (9) and (24) indicated below.
4. ☐ The US has been elected by the expiration of 19 months from the priority date (Article 31).
5. ☒ A copy of the International Application as filed (35 U.S.C. 371 (c) (2))
   - a. ☐ is attached hereto (required only if not communicated by the International Bureau).
   - b. ☒ has been communicated by the International Bureau.
   - c. ☐ is not required, as the application was filed in the United States Receiving Office (RO/US).
6. ☒ An English language translation of the International Application as filed (35 U.S.C. 371(c)(2)).
   - a. ☒ is attached hereto.
   - b. ☐ has been previously submitted under 35 U.S.C. 154(d)(4).
7. ☒ Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. 371 (c)(3))
   - a. ☐ are attached hereto (required only if not communicated by the International Bureau).
   - b. ☐ have been communicated by the International Bureau.
   - c. ☐ have not been made; however, the time limit for making such amendments has NOT expired.
   - d. ☒ have not been made and will not be made.
8. ☐ An English language translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371(c)(3)).
9. ☐ An oath or declaration of the inventor(s) (35 U.S.C. 371 (c)(4)).
10. ☐ An English language translation of the annexes of the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371 (c)(5)).
11. ☐ A copy of the International Preliminary Examination Report (PCT/IPEA/409).
12. ☐ A copy of the International Search Report (PCT/ISA/210).

Items 13 to 20 below concern document(s) or information included:

13. ☐ An Information Disclosure Statement under 37 CFR 1.97 and 1.98.
14. ☐ An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included.
15. ☒ A **FIRST** preliminary amendment.
16. ☐ A **SECOND** or **SUBSEQUENT** preliminary amendment.
17. ☐ A substitute specification.
18. ☐ A change of power of attorney and/or address letter.
19. ☐ A computer-readable form of the sequence listing in accordance with PCT Rule 13ter.2 and 35 U.S.C. 1.821 - 1.825.
20. ☐ A second copy of the published international application under 35 U.S.C. 154(d)(4).
21. ☐ A second copy of the English language translation of the international application under 35 U.S.C. 154(d)(4).
22. ☒ Certificate of Mailing by Express Mail
23. ☐ Other items or information:

JC18 Rec'd PCT/PTO 13 JUL 2001

U.S. APPLICATION NO. (IF KNOWN, SEE 37 CFR 09/889260	INTERNATIONAL APPLICATION NO. PCT/DE00/00021	ATTORNEY'S DOCKET NUMBER 83256

				CALCULATIONS	PTO USE ONLY
24. The following fees are submitted:.					
BASIC NATIONAL FEE (37 CFR 1.492 (a) (1) - (5)) :					
☐ Neither international preliminary examination fee (37 CFR 1.482) nor international search fee (37 CFR 1.445(a)(2)) paid to USPTO and International Search Report not prepared by the EPO or JPO **$1000.00**					
☒ International preliminary examination fee (37 CFR 1.482) not paid to USPTO but International Search Report prepared by the EPO or JPO **$860.00**					
☐ International preliminary examination fee (37 CFR 1.482) not paid to USPTO but international search fee (37 CFR 1.445(a)(2)) paid to USPTO **$710.00**					
☐ International preliminary examination fee (37 CFR 1.482) paid to USPTO but all claims did not satisfy provisions of PCT Article 33(1)-(4) **$690.00**					
☐ International preliminary examination fee (37 CFR 1.482) paid to USPTO and all claims satisfied provisions of PCT Article 33(1)-(4) **$100.00**					
ENTER APPROPRIATE BASIC FEE AMOUNT =				**$860.00**	
Surcharge of **$130.00** for furnishing the oath or declaration later than ☐ 20 ☒ 30 months from the earliest claimed priority date (37 CFR 1.492 (e)).				**$130.00**	
CLAIMS	NUMBER FILED	NUMBER EXTRA	RATE		
Total claims	4 - 20 =	0	x $18.00	**$0.00**	
Independent claims	1 - 3 =	0	x $80.00	**$0.00**	
Multiple Dependent Claims **(check if applicable).**			☐	**$0.00**	
TOTAL OF ABOVE CALCULATIONS =				**$990.00**	
☐ Applicant claims small entity status. (See 37 CFR 1.27). The fees indicated above are reduced by 1/2.				**$0.00**	
SUBTOTAL =				**$990.00**	
Processing fee of **$130.00** for furnishing the English translation later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 CFR 1.492 (f)). +				**$0.00**	
TOTAL NATIONAL FEE =				**$990.00**	
Fee for recording the enclosed assignment (37 CFR 1.21(h)). The assignment must be accompanied by an appropriate cover sheet (37 CFR 3.28, 3.31) **(check if applicable).** ☐				**$0.00**	
TOTAL FEES ENCLOSED =				**$990.00**	
				Amount to be: refunded	$
				charged	$

a. ☒ A check in the amount of **$990.00** to cover the above fees is enclosed.

b. ☐ Please charge my Deposit Account No. ______________ in the amount of ______________ to cover the above fees. A duplicate copy of this sheet is enclosed.

c. ☒ The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to Deposit Account No. **23-0920** A duplicate copy of this sheet is enclosed.

d. ☐ Fees are to be charged to a credit card. **WARNING:** Information on this form may become public. **Credit card information should not be included on this form.** Provide credit card information and authorization on PTO-2038.

NOTE: Where an appropriate time limit under 37 CFR 1.494 or 1.495 has not been met, a petition to revive (37 CFR 1.137(a) or (b)) must be filed and granted to restore the application to pending status.

SEND ALL CORRESPONDENCE TO:

Gerald T. Shekleton, Esq.
WELSH & KATZ, LTD.
120 S. Riverside Plaza
22nd Floor
Chicago, Illinois 60606

Gerald T. Shekleton

SIGNATURE

Gerald T. Shekleton

NAME

27,466

REGISTRATION NUMBER

7/13/01

DATE

09/889260

CERTIFICATE OF MAILING BY "EXPRESS MAIL" (37 CFR 1.10) Applicant(s): **Infineon Technologies AG**	JC18 Rec'd PCT/PTO 13 JUL 2001 Docket No. **83256**

Serial No.	Filing Date	Examiner	Group Art Unit

Invention: **ELECTRONIC PHASE-LOCKED LOOP**

I hereby certify that the following correspondence:

Section 371 Patent Application

(Identify type of correspondence)

is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 CFR 1.10 in an envelope addressed to: The Assistant Commissioner for Patents, Washington, D.C. 20231 on

____
(Date)

Fred Franks
(Typed or Printed Name of Person Mailing Correspondence)

Fred Franks
(Signature of Person Mailing Correspondence)

EL432086573US
("Express Mail" Mailing Label Number)

09889260 .071302

Note: Each paper must have its own certificate of mailing.

P06A/REV02

83256 PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re U.S. Patent Application	)
Applicant: Infineon Technologies	)
Serial No.: Not Yet Assigned	)
Filed: Herewith	)
For: ELECTRONIC PHASE-LOCKED LOOP	)

PRELIMINARY AMENDMENT

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

This is a Preliminary Amendment for entry in the above-identified application.

In the Claims:

Please amend the claims as follows:

1. (amended) An electronic phase-locked loop for jitter-attenuated clock multiplication, in particular as part of an integrated circuit for integrated services communications networks, data communication or networks in which the frequency of a controllable oscillator is set in such a way that it corresponds to a reference frequency, the output signal of the oscillator being compared with the reference frequency in a digital phase detector, and the output signal of the digital phase detector setting the frequency of the oscillator via a digital regulated system, wherein the digital phase-locked loop is connected up to an additional analog phase detector and a lock detection for activation.

2. (amended) The electronic phase-locked loop as claimed in claim 1, wherein that the digital phase-locked loop comprises a digital phase detector, a code converter, a PI filter, a drive circuit for the oscillator, the oscillator, which is designed as a digitally controllable crystal oscillator, and a counter, the lock detection being undertaken by the code converter.

3. (amended) The electronic phase-locked loop as claimed in claim 1, wherein by a configuration such that, in the event of transition of the digital phase-locked loop into a limit cycle with a phase error, called jitter, alternating between accuracy is canceled by the additional analog phase detector, the lock detection activating the analog phase detector via a line, said analog phase detector thereupon regulating both clock edges of the jitter in a continuously variable manner until said clock edges are synchronous with one another.

4. (amended) An integrated circuit having an electronic phase-locked loop of claim 1.

<u>IN THE SPECIFICATION:</u>

Please add the attached Abstract to the specification.

Respectfully submitted,

WELSH & KATZ, LTD.

By

Gerald T. Shekleton
Registration No. 27,466

Dated: July 13, 2001

Welsh & Katz, Ltd.
120 South Riverside Plaza, 22nd Floor
Chicago, Illinois 60606
Telephone: 312/655-1500

VERSION WITH MARKINGS TO SHOW CHANGES MADE

1. (amended) An electronic phase-locked loop [(PLL)] for jitter-attenuated clock multiplication, in particular as part of an integrated circuit [(IC)] for integrated services communications networks [(ISDN)], data communication or networks in which the frequency of a controllable oscillator [(9, DCXO)] is set in such a way that it corresponds to a reference frequency [(REF CLK)], the output signal of the oscillator [(DCXO CLK)] being compared with the reference frequency in a digital phase detector [(1)], and the output signal of the digital phase detector [(1)] setting the frequency of the oscillator [(9)] via a digital regulated system, [characterized in that] wherein the digital phase-locked loop is connected up to an additional analog phase detector [(2, APD)] and a lock detection [(4)] for activation.

2. (amended) The electronic phase-locked loop ([PLL)] as claimed in claim 1, [characterized in that] wherein the digital phase-locked loop comprises a digital phase detector [(1)], a code converter [(4)], a PI filter [(10)], a drive circuit [(8, DCXO-control)] for the oscillator [(9)], the oscillator [(9, DCXO)], which is designed as a digitally controllable crystal oscillator, and a counter [(3)], the lock detection being undertaken by the code converter[(4)].

3. (amended) The electronic phase-locked loop [(PLL)] as claimed in claim[s] 1 [or 2, characterized by] wherein a configuration such that, in the event of transition of the digital phase-locked loop into a limit cycle with a phase error, called jitter, alternating between accuracy is canceled by the additional analog phase detector [(2)], the lock detection activating the analog phase detector [(2)] via a line [(10, "ana_mode")], said analog phase detector

thereupon regulating both clock edges of the jitter in a continuously variable manner until said clock edges are synchronous with one another.

4. (amended) An integrated circuit [(IC)] having an electronic phase-locked loop [(PLL)] of claim[s] 1[, 2 or 3].

09/889260
JC18 Rec'd PCT/PTO 13 JUL 2001

5JPR75

Description

Electronic phase-locked loop (PLL)

The invention relates to an electronic phase-locked loop (PLL) for jitter-attenuated clock multiplication, in particular as part of an integrated circuit (IC) for integrated services communications networks (ISDN), data communication or networks.

In the prior art, it is customary for the frequency to be set in such a way that it corresponds to a reference frequency. For this purpose, analog circuit arrangements have a controllable oscillator whose output signal is compared with the reference frequency in a phase detector. The output signal of the analog phase detector in turn sets the frequency of the controllable oscillator via a regulated system. An analog circuit arrangement of this type is generally more difficult to integrate than a digital circuit arrangement and usually requires additional components. The regulation is fairly accurate.

A digital implementation of a phase-locked loop is simple to integrate, affords the possibilities of rapid conversion to new technologies by using synthesis tools, and is relatively independent of fluctuations in the process for fabricating the integrated circuit (IC). The regulating accuracy can be achieved right down to the lowest discretization level for the digital representation of the numerical values.

One disadvantage of the digital PLL that has been customary heretofore is that, on account of inherent quantization, the PLL undergoes transition into a so-called "limit cycle" and henceforth alternates between a phase error of +1, 0 and -1; as a result, the high-

frequency clock signal generated has a slow but unavoidable variance, called "jitter".

In the publication relating to the conference "IEEE 1988 CUSTOM INTEGRATED CIRCUITS CONFERENCE", CH2584-1/88/0000-0051, pages 9.5.1 to 9.5.3, a description is given, by Rockwell International Semiconductor Products Division, i.e. by the authors Shi & al., of an electronic circuit arrangement designated "Jitter Attenuation Phase Locked Loop using switched capacitor controlled crystal oscillator", which is intended to effect jitter attenuation.

A phase-locked loop (PLL) is used which attenuates jitter amplitudes of up to 30 unit intervals (UI) at a bandwidth of less than 2 Hz. The PLL has a crystal oscillator which is controlled in three frequencies by switched capacitors, and a down-counting sequential logic phase/frequency detector. By dynamic variation of the charging capacitance, the frequency of the oscillator is adjusted in accordance with the operating cycle of the control signal. Digital CMOS technology is used in this case. This technology does not require a complicated analog circuit. The digital control logic is simple.

DE-A1-39 20 008 describes an electronic phase-locked loop (PLL) appertaining to communications and data technology which has a phase comparator and an oscillator controlled by means of a switching matrix designed as capacitance or inductance matrix. The frequency of the oscillator can be set precisely, over the accuracy values that are limited by the tolerance limits of the switching matrix, by virtue of the fact that at least one switching element, preferably the least significant one, of the switching matrix is driven by a pulse length modulator. A first output signal burst formed by a microprocessor is fed to the

switching matrix, and at least one further output signal burst is applied to the pulse length modulator. The pulse length modulator is clocked by a clock signal derived from an output signal of the voltage-controlled oscillator, said clock signal also driving a switch for driving the switching element.

Consequently, just like in the PLL according to the IEEE Conference publication discussed above, what is present is digital, in this case additionally refined, stepwise control of the oscillator which, moreover, certainly helps to reduce the so-called jitter, even though such "jitter" is not mentioned per se.

Against the background of this prior art, the invention is based on the object of attenuating, in an electronic phase-locked loop (PLL) of digital design, even the jitter of the lowest digital discretization level.

This object is achieved according to the invention by means of the subject matter of the independent patent claims 1 and 4, respectively. Further refinements are characterized in the dependent patent claims 2 and 3.

The invention provides a digital phase-locked loop - which can be synthesized from standard cells - with the assistance of an analog phase detector and a circuit for lock detection, whereby the disadvantages hitherto of the purely digital solution are overcome.

The invention is explained in more detail below in an exemplary embodiment and with reference to the drawings.

Fig. 1 shows a phase-locked loop PLL with digital regulation and with an additional analog phase detector APD being incorporated according to the invention;

Fig. 2 illustrates the profile of the driving of the oscillator DCXO from the drive circuit DCXO-control within a conventional digital PLL;

Fig. 3 shows the jitter in the output signal of the phase detector DPD in a conventional digital PLL;

Fig. 4 diagrammatically shows the operation of the analog phase detector APD in the PLL according to the invention; and

Fig. 5 shows an illustration of the regulation according to the invention using a simulation example.

Fig. 1 shows the block diagram of the phase-locked loop PLL configured according to the invention, comprising two phase detectors, namely the digital DPD 1 and the additional analog phase detector APD 2, and also a code converter 4, which undertakes, inter alia, the lock detection, a PI filter or PI regulator 10, which comprises, in a known manner, an integral regulation 5 and also a linear regulation 6, and also an addition and amplifier stage 7, and a driver DCXO-control 8 for the oscillator, a digitally controllable crystal oscillator DCXO 9, and also a counter 3. In the example, the counter 3 operates like a divider with the divisor 2048, an exemplary 8 kHz clock frequency resulting from the division of 16.384 MHz by 2048, which are fed into the DPD 1 in addition to a reference frequency of 8 kHz.

The method of operation of the digital PLL is as follows and is illustrated in Figures 2 and 3, the reference clock signal REF-CLK being illustrated in relation to the content of the counter 3:

Upon each rising edge of the reference clock signal (REF-CLK), the present value of the counter 3 is stored in the phase detector 1 (see Fig. 2) and is applied to the PI filter 5, 6 via the code converter 4. In this case, the counter reading is a measure of the phase error and can be positive or negative. This quantized phase error is fed via the PI filter 5, 6 to the oscillator 9, which is thereby either slowed down or accelerated. In other words, in the left-hand part of Fig. 2, the oscillator 9 must be accelerated, while it is synchronous with the reference clock signal in the middle part. In the right-hand part of Fig. 2, the oscillator 9 is too fast and must be slowed down. In this way, the zero crossing of the counter 3, which acts like a clock divider, is regulated in the direction of the rising edge of the reference clock signal. If the counter reading that is found is equal to zero, the PLL has locked on, i.e. the high-frequency clock signal generated and the reference clock signal are phase-synchronous.

As mentioned in the introduction, one disadvantage of the digital solution, as can be seen from the simulation in Fig. 3, is that the PLL undergoes transition into a so-called "limit cycle" with variance of the clock signal as "jitter".

The above-indicated limitation of the accuracy is cancelled by the invention's augmentation of the existing phase-locked loop (PLL) by the analog phase detector (2, APD) (see Fig. 4). If the digital phase-locked loop has regulated the two clock edges in a synchronous manner to an extent such that the phase error applied to the code converter is zero, a lock detection activates the additional analog phase detector APD 2 via a line "ana_mode" (also see Fig. 5). Said analog phase detector regulates in a continuously

variable manner until both clock edges are fully synchronous. In this case, by generating a so-called "double zero" around which regulation is effected, the code converter 4 ensures that the APD 2 actually remains activated once it has been so activated. Only in the event of relatively large phase differences is the analog phase detector 2 deactivated, and renewed digital coarse regulation takes place.

Further comments with respect to the figures are, specifically:

In Fig. 2, the profiles of the reference clock signal REF-CLK are plotted against the values of the counter 3. The illustration on the left-hand side shows an oscillator DCXO 9 that is too slow. It should be accelerated, i.e. the capacitance charge (CAP LOAD) should be reduced. The middle illustration shows a DCXO 9 in synchronization with REF-CLK. The speed should be maintained, i.e. no change in capacitance (CAPS). The illustration on the right-hand side illustrates a DCXO 9 that is too fast. The capacitance charge should be increased.

Owing to the inherent "quantization error", the PLL will jump between -1, 0 and +1, and in the opposite order.

In the top and bottom graphs, Fig. 3 uses simulation results to show how a digital phase detector 1, DPD operates and the jitter is manifested as an oscillation. The counting frequency or the counting time is plotted on the abscissa and the regulating amplitude is plotted on the ordinate. Thus, the result of the digital phase detector DDP 1 is illustrated at point 20, whose result fluctuates between -1, 0 and +1. The other two curves show the profile of the output signal of the PI filter 10 and of the signal FCTRL of

the oscillator control DCXO-control 9. This quantized phase error effects a slow jitter in the difference between clock signal CLK and reference clock signal REF-CLK, illustrated in the bottom part of Fig. 3 by the curve connected to 22 by the arrow, and also a fast jitter in the clock signal CLK at 21. In this case, V denotes the difference and Hz correspondingly denotes the frequency.

Fig. 4 illustrates the operation of the analog phase detector 2 added according to the invention. According to the block diagram, the clock frequency from the oscillator 9 is applied to one input of the analog phase detector 2 and the reference clock signal of 8 kHz is applied to the other input. The counter result and the same 8 kHz reference clock signal are fed into the input of the digital phase detector, whose output is connected to the input of the code converter 4. From the code converter 4, a line "ana_mode" passes to a third input of the analog phase detector 2. A signal for reducing the speed of the oscillator 9 then leaves the analog phase detector 2.

The illustration of the phase relationships shows, in the first graph, the clock signal DCXO CLK leading the reference clock signal REF CLK. Acceleration of the DCXO 9 is required in this case. In the second graph, the clock signal DCXO CLK lags behind the clock signal REF CLK, with the result that the DCXO 9 must be slowed down. Thus, the two clock edges are brought to coincidence according to the invention.

Fig. 5 shows how the time difference in ns between the 8 kHz input clock signal and the 8 kHz output clock signal is manifested, and where the analog phase detector 2 joins in, whereupon the phase difference between the two clock signals is reduced to approximately 0 ns. Abscissa and ordinate are graduated

in accordance with Fig. 3. The time difference between the output clock signal CLK of the oscillator 9 and the reference clock signal REF-CLK is illustrated in 22, while the analog phase detector APD 2 locks on. Likewise, the difference between the clock signals is regulated to 0 in 24. The scaling of the frequency has been omitted in Fig. 5.

Patent claims

1. An electronic phase-locked loop (PLL) for jitter-attenuated clock multiplication, in particular as part of an integrated circuit (IC) for integrated services communications networks (ISDN), data communication or networks in which the frequency of a controllable oscillator (9, DCXO) is set in such a way that it corresponds to a reference frequency (REF CLK), the output signal of the oscillator (DCXO CLK) being compared with the reference frequency in a digital phase detector (1), and the output signal of the digital phase detector (1) setting the frequency of the oscillator (9) via a digital regulated system, characterized in that
the digital phase-locked loop is connected up to an additional analog phase detector (2, APD) and a lock detection (4) for activation.

2. The electronic phase-locked loop (PLL) as claimed in claim 1, characterized in that the digital phase-locked loop comprises a digital phase detector (1), a code converter (4), a PI filter (10), a drive circuit (8, DCXO-control) for the oscillator (9), the oscillator (9, DCXO), which is designed as a digitally controllable crystal oscillator, and a counter (3), the lock detection being undertaken by the code converter (4).

3. The electronic phase-locked loop (PLL) as claimed in claims 1 or 2, characterized by a configuration such that, in the event of transition of the digital phase-locked loop into a limit cycle with a phase error, called jitter, alternating between the values +1, 0 and -1, the limitation of the accuracy is cancelled by the additional analog phase detector (2), the lock detection activating

the analog phase detector (2) via a line (10, "ana_mode"), said analog phase detector thereupon regulating both clock edges of the jitter in a continuously variable manner until said clock edges are synchronous with one another.

4. An integrated circuit (IC) having an electronic phase-locked loop (PLL) of claims 1, 2 or 3.

09/889260

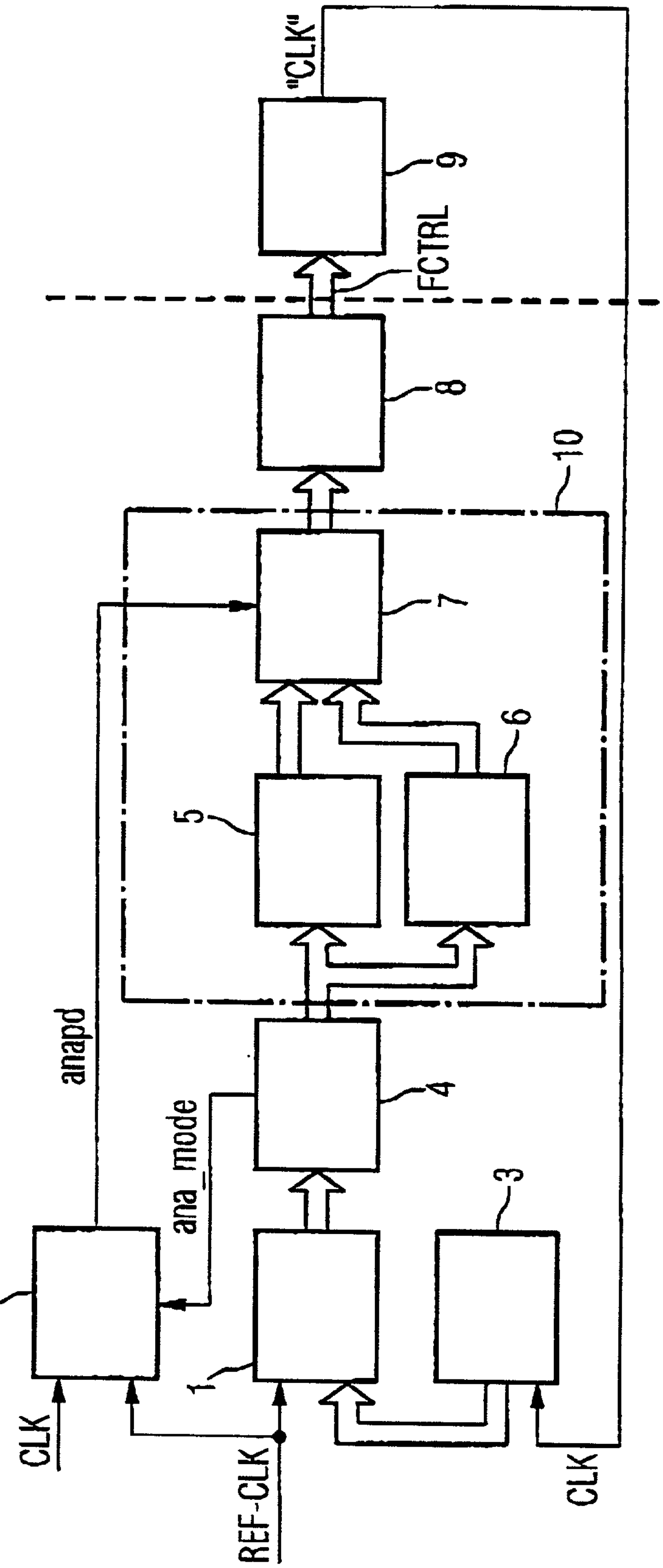


FIG 1

09/889260

2/5

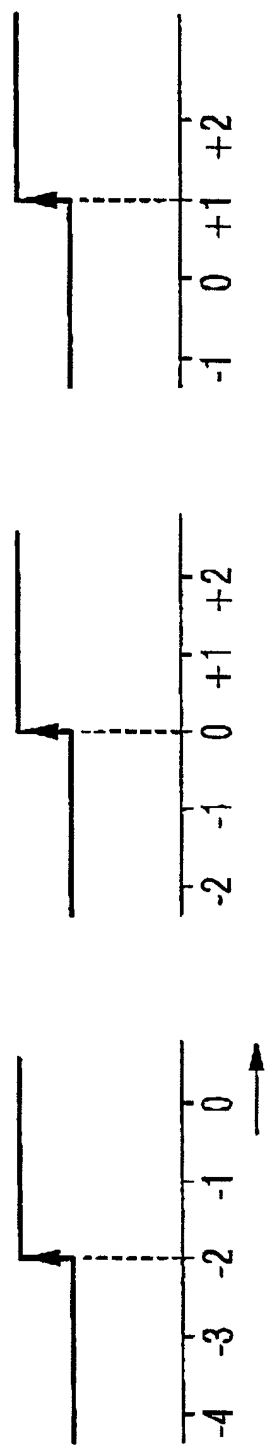


FIG 2

09/889260

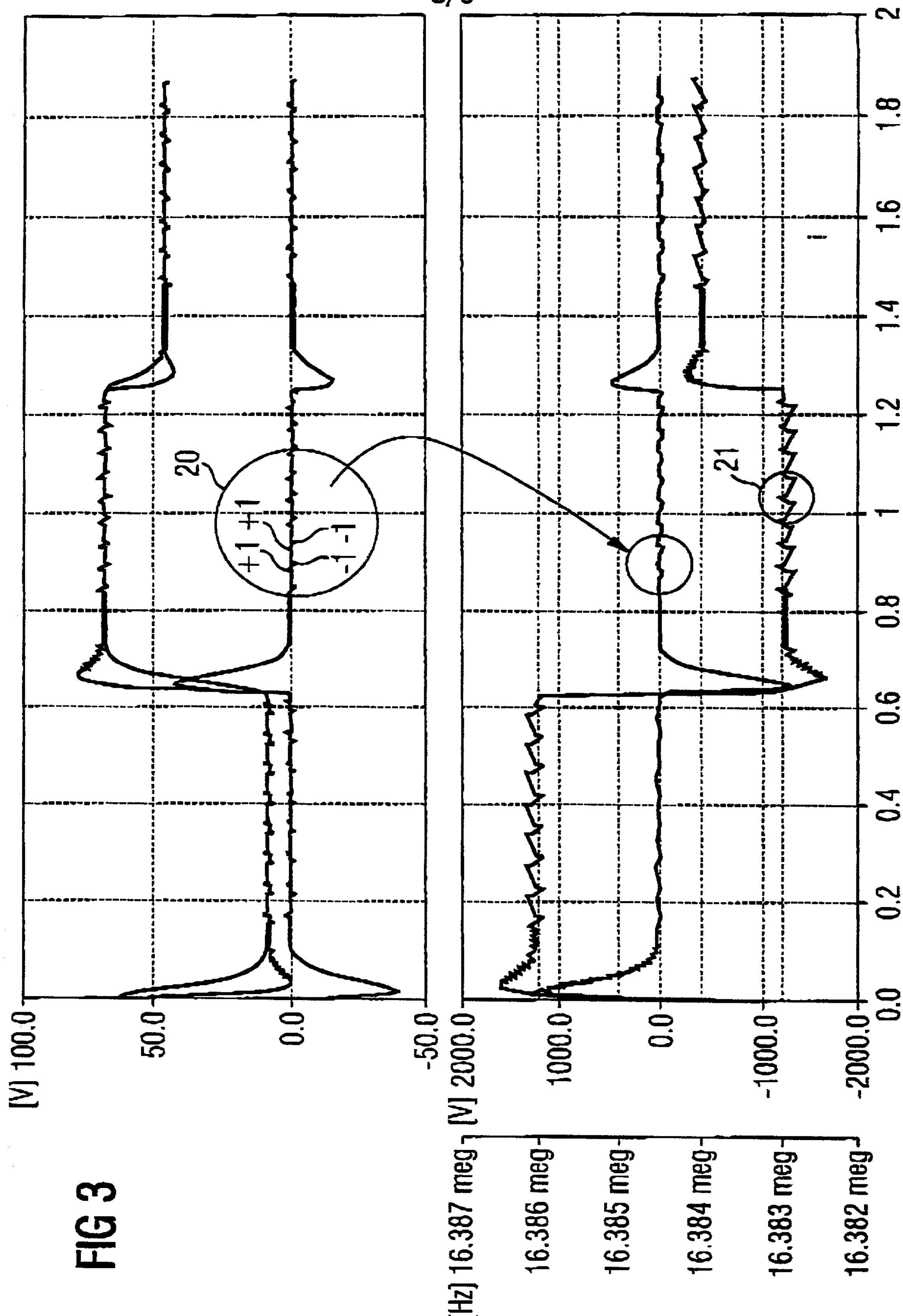
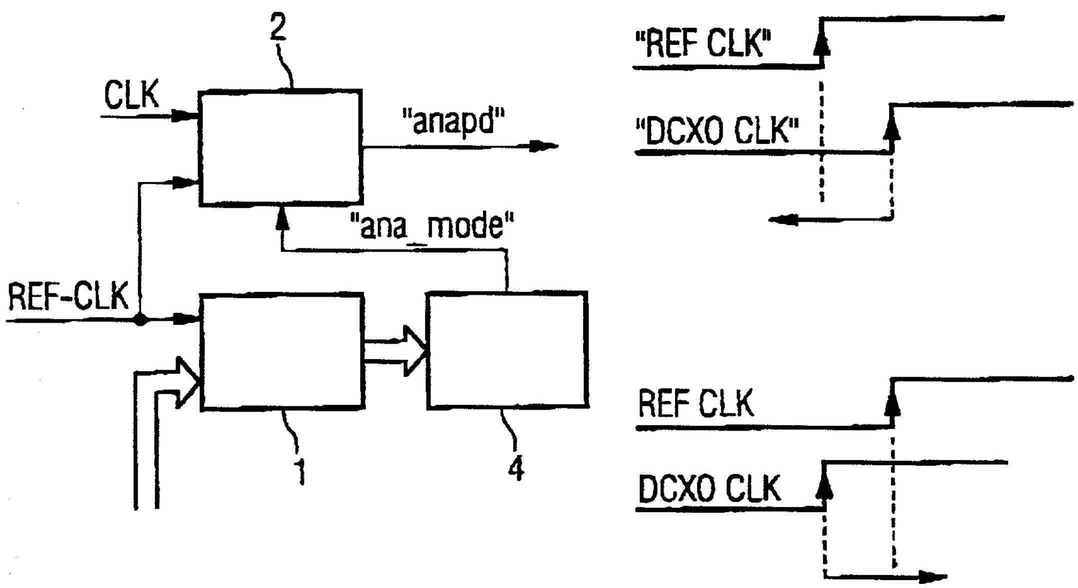


FIG 3

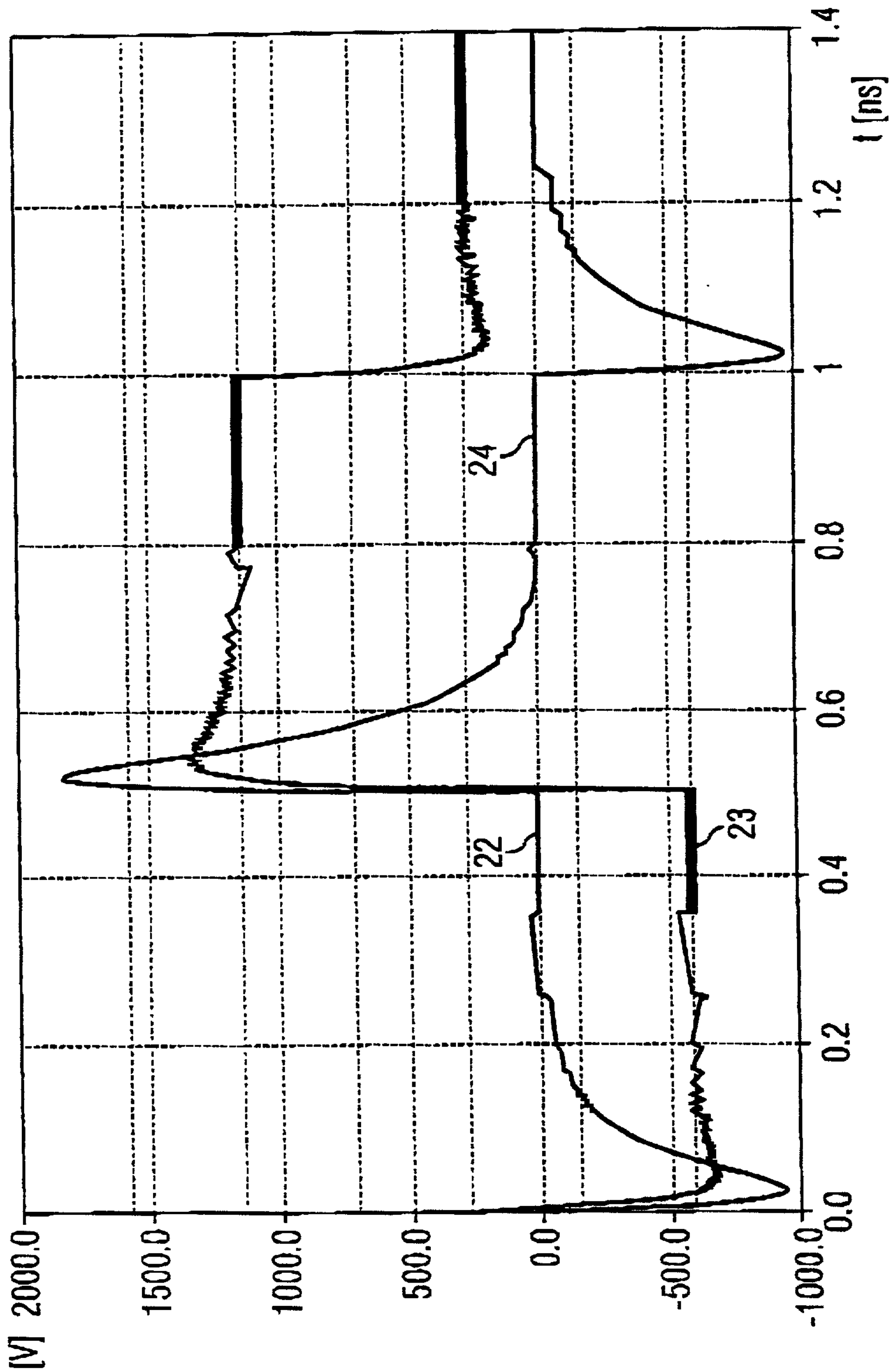
09/889260

FIG 4



09/889260

FIG 5



DECLARATION AND POWER OF ATTORNEY

As a below named inventor, I hereby declare:

That my residence, post office address and citizenship are as stated below next to my name.

That I verily believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural inventors are named below) of the subject matter which is claimed and for which a patent is sought on the invention entitled: **ELECTRONIC PHASE-LOCKED LOOP** the specification of which (check one)

☒ is attached hereto.

☐ was filed on as Application, Serial No. and was amended on ________________ (if applicable).

That I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

That I acknowledge the duty to disclose information known to be material to patentability of this application in accordance with Title 37, Code of Federal Regulations §1.56(a).

That I hereby claim foreign priority benefits under Title 35, United States Code, §119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate on this invention having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s)

(Number)	(Country)	(Day/Month/Year Filed)	Priority Claimed
199 02 335.2	Germany	21 January 1999	☒ Yes ☐ No
WO 00/43849	PCT	01 January 2000	☒ Yes ☐ No

That I hereby claim the benefit under Title 35, United States Code, §120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, §1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

United States Application(s)

(Application Serial No.)	(Filing Date)	(Status)-(Patented, pending, abandoned)

That all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18

That all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

I hereby appoint the following attorneys, with full power of substitution and revocation, to prosecute this application and to transact all business in the United States Patent and Trademark Office connected therewith and request that all correspondence and telephone calls in respect to this application be directed to: WELSH & KATZ, LTD., 120 South Riverside Plaza, 22nd Floor, Chicago, Illinois 60606-3913, Telephone No.: (312) 655-1500:

Attorney	Registration No.
A. Sidney Katz	24,003
Richard L. Wood	22,839
Jerold B. Schnayer	28,903
Eric C. Cohen	27,429
Joseph R. Marcus	25,060
Gerald S. Schur	22,053
Gerald T. Shekleton	27,466
James A. Scheer	29,434
Daniel R. Cherry	29,054
Edward P. Gamson	29,381
Kathleen A. Rheintgen	34,044
Thomas W. Tolpin	27,600

I hereby authorize the U.S. attorney or agent named herein to accept and follow instructions from Reinhard Skuhra Weise & Partner as to any action to be taken in the Patent and Trademark Office regarding this application without direct communication between the U.S. attorney or agent and the undersigned. In the event of a change in the persons from whom instructions may be taken, I will so notify the U.S. attorney or agent named herein.

Full name of sole or one joint inventor: Siegfried HART

Inventor's signature: Siegfried Hart

Date: September 18, 2001

Residence and Post Office Address: Mitterweg 7

83620 ~~Kleinhochenrain~~ Germany DEX

Citizenship: German

Full name of sole or one joint inventor: Heinz WERKER

Inventor's signature: Heinz Werker

Date: 22.09.2001

Residence and Post Office Address: Ringstr. 10

82386 Huglfing Germany

Citizenship: German

Address for Correspondence:

WELSH & KATZ, LTD.
120 South Riverside Plaza
22nd Floor
Chicago, Illinois 60606-3913

09889250.040302